

Listing of Claims:

1. (Original) An electronic device comprising:
an element of chalcogenic material;
a control circuit coupled to chalcogenic element; and
a temperature detection circuit coupled to the control circuit, the temperature detection circuit including a sense resistor of chalcogenic material and being structured to control the control circuit based on a temperature sensed by the sense resistor.
2. (Original) A device according to claim 1, wherein said element of chalcogenic material is a phase change storage element and said device is a phase change non-volatile memory device.
3. (Original) A device according to claim 2, wherein said sense resistor of chalcogenic material and said phase change storage element have the same structure.
4. (Original) A device according to claim 1, wherein said sense resistor of chalcogenic material generates an electrical quantity tracing with the temperature, the device further comprising a processor receiving said electrical quantity and generating a reference quantity tracing with temperature, and passing the reference quantity to the control circuit.
5. (Original) A device according to claim 4, wherein said processor comprises an analog-to-digital converter receiving said electrical quantity and generating a digital word correlated to temperature and a reference quantity generator receiving said digital word and generating said reference quantity.
6. (Original) A device according to claim 5, wherein said reference quantity generator is a voltage regulator having a control input receiving said digital word.

7. (Original) A device according to claim 6, wherein said voltage regulator comprises an operational amplifier having an input and an output and a feedback resistive network connected between said input and said output of said operational amplifier; said resistive network comprising a controllable resistor having a control input receiving said digital word.

8. (Original) A device according to claim 4, wherein said processor comprises a voltage regulator.

9. (Original) A device according to claim 8, wherein said voltage regulator comprises an operational amplifier having a first and a second input and an output and a feedback resistive network connected between said first input and said output of said operational amplifier, said second input of said operational amplifier being connected to said sense resistor of chalcogenic material.

10. (Original) A device according to claim 4, wherein said processor comprises a current source.

11. (Original) A device according to claim 4 wherein the chalcogenic element is a phase change storage element and the control circuit is a biasing circuit receiving said reference quantity and generating a biasing quantity for said phase change storage element.

12. (Original) A device according to claim 11, further comprising a write selection circuit connecting said control circuit to said phase change storage element to supply said phase change storage element with a current pulse having an amplitude that varies with the temperature.

13. (Original) A device according to claim 1, wherein said temperature detection circuit comprises an operational amplifier having an input and an output and a feedback resistive network connected between said input and said output of said operational amplifier; said resistive network including said sense resistor of chalcogenic material.

14. (Original) A device according to claim 1 wherein said element of chalcogenic material is a phase change storage element, said device is a phase change non-volatile memory device, and the control circuit is a read circuit for reading the storage element by comparing a reference quantity tracing with the sensed temperature to a read quantity that reflects a logical status of the storage element.

15. (Original) A method for tracing temperature in an electronic device including an element of chalcogenic material, the method comprising:

detecting an existing temperature through a sense resistor of chalcogenic material;

and

controlling the chalcogenic element based on the temperature detected by the sense resistor.

16. (Original) A method according to claim 15, wherein said electronic device comprises a phase change storage element that includes the chalcogenic element.

17. (Original) A method according to claim 16, wherein the phase change storage device is a non-volatile memory, further comprising the steps of:

generating an electrical quantity tracing with temperature; and

processing said electrical quantity to generate a reference quantity tracing with temperature.

18. (Original) A method according to claim 17, wherein said step of generating comprises generating one between a reference voltage and a reference current.

19. (Original) A method according to claim 18, wherein the controlling step includes:

generating a write biasing current correlated to said reference current; and

supplying said write biasing current to said phase change memory cell.

20. (Original) A method according to claim 18, wherein the controlling step includes:

generating a read biasing current correlated to said reference current; and
supplying said read biasing current to said phase change memory cell.

21. (Original) A method according to claim 16 wherein the controlling step includes reading the storage element by:

receiving from the storage element an electrical read quantity that reflects a logical status of the storage element;

generating an electrical reference quantity that depends on the temperature detected by the sense resistor; and

comparing the electrical read quantity to the electrical reference quantity to determine the logical status of the storage element.

22. (Original) A memory device, comprising:

a memory array of phase-change memory elements each including a chalcogenic element;

a control circuit coupled to the memory array; and

a temperature detection circuit coupled to the control circuit, the temperature detection circuit including a sense resistor of chalcogenic material and being structured to control the control circuit based on a temperature sensed by the sense resistor.

23. (Original) The memory device of claim 22 wherein the sense resistor and each memory element have substantially the same structure.

24. (Original) The memory device of claim 22, wherein the sense resistor generates an electrical quantity tracing with the temperature, the device further comprising a processor receiving the electrical quantity and generating a reference quantity tracing with temperature, and passing the reference quantity to the control circuit.

25. (Original) The memory device of claim 24, wherein the processor comprises an analog-to-digital converter receiving the electrical quantity and generating a digital word correlated to temperature and a reference quantity generator receiving the digital word and generating the reference quantity.

26. (Original) The memory device of claim 24, wherein the processor includes a voltage regulator that generates the reference quantity.

27. (Original) The memory device of claim 26, wherein the voltage regulator comprises an operational amplifier having an input and an output and a feedback resistive network connected between the input and the output of the operational amplifier; the resistive network comprising a controllable resistor that is controlled based on the temperature sensed by the sense resistor.

28. (Original) The memory device of claim 27 wherein the voltage regulator comprises an operational amplifier having a first and a second input and an output and a feedback resistive network connected between the first input and the output of the operational amplifier, the second input of the operational amplifier being connected to the sense resistor.

29. (Original) The memory device of claim 22, further comprising a write selection circuit connecting the biasing circuit to each of the phase change storage elements to supply the phase change storage elements with a current pulse having an amplitude that varies with the temperature.

30. (Original) The memory device of claim 22, wherein the temperature detection circuit comprises an operational amplifier having an input and an output and a feedback resistive network connected between the input and the output of the operational amplifier; the resistive network including the sense resistor.

31. (Original) The memory device of claim 22 wherein the control circuit is a read circuit for reading the storage elements by comparing a reference quantity tracing with the sensed temperature to a read quantity that reflects a logical status of one of the storage elements.